UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/761,538	01/16/2001	William J. Dally	2789.2005-002	5874

24319 7590 02/07/2007

LSI LOGIC CORPORATION
1621 BARBER LANE
MS: D-106
MILPITAS, CA 95035

EXAMINER	
CHANG, RICHARD	
ART UNIT	PAPER NUMBER
2616	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/761,538	DALLY, WILLIAM J.	
	Examiner	Art Unit	
	Richard Chang	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-20,22-52 and 54-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-4,6-20,22-36,54,57 and 58* is/are allowed.

6)☒ Claim(s) *37-52* is/are rejected.

7)☒ Claim(s) *55 and 56* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01/16/2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to arguments

1. Applicant's arguments and amendment, filed on 01/17/2007, with respect to claims 37-52 have been fully considered and but are not persuasive. The following comments fully address applicant's argument with respect to the rejection.

The finality of the last action is withdrawn.

Claims 5, 21 and 53 had been canceled.

-- In response to applicant's argument that the cited reference does not support the limitation of "plural switches on plural chips" and "switches of different stages being on common chips" (See Applicant's Remarks, page 1, paragraph 2) in claim 37. The cited references teaches the functions and performances of switches of different stage performed independent in a form of structure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the switching functions of different stages into a single chip integral form or multiple common chips form to perform the same functions of plural switches of different stages which is merely a matter of obvious engineering choice since it has been held by In re Larson, 340 F.2d 965, 968. 144 USPQ 347, 349 (CCPA 1965).

-- In response to applicant's argument that the cited reference does not support the limitation of "a first frame counter and a second frame counter" (See Applicant's Remarks, page 1, paragraph 2) in claim 41. Ohara further teaches that there is at least

one counter receiving as input the timing pulse in each input side interface unit to maintain the frame synchronization for related portions of input data frames (See Fig. 4, Col. 6, lines 18-30). Furthermore, there are multiple each input side interface units to maintain the frame synchronization for related portions of input data frames. As such the limitation in claim 41 is met.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 37-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent No. 6,693,902 ("Sahlman et al.") in view of U.S. Patent No. 6,243,361 ("McMillen et al.") and further in view of U.S. Patent No. 5,144,297 ("Ohara").

Regarding claims 37 and 41, Sahlman et al. teach a digital cross connect (a Cross-connection architecture for SDH signals) comprising

plural switching stages, each stage having plural switches receiving plural frames of time multiplexed input data and switching the data in time and space (a SDH frame based time-and-space division switch groups where time switch realizes the rearrangement of the time slots or bytes in accordance with the route selection calculated by the decoder processor control before they are transmitted to the space switch),

wherein configuration switching is initiated by a prepare-to-switch signal propagated from a master switch to all switches of an output stage and the input stage, the at least one switch then propagating the configuration select signal (an SDH DXC can transmit traffic between different SDH levels and connect traffic between different signals and the use of the cross connect also includes a possibility for remote control of routing, initialization of reserve routes, connection from one signal to several signals) (See Fig. 1, Col. 4, line 62 to Col. 6, line 36).

Furthermore, the cited references teaches the functions and performances of switches of different stage performed independent in a form of structure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the switching functions of different stages into a single chip integral form or multiple common chips form to perform the same functions of plural switches of different stages which is merely a matter of obvious engineering choice since it has been held by In re Larson, 340 F.2d 965, 968. 144 USPQ 347, 349 (CCPA 1965).

Sahlman et al. teach substantially all the claimed invention but did not disclose expressly the particular application involving limitations of

"configuration storage at each switch storing a time/space configuration for the switch" and

"all switches switching configuration to the stored time/space configuration in frame synchronization at the start of synchronized data frames by synchronizing switches of successive stages to a configuration select signal propagated from at least one switch of an input stage".

McMillen et al. teach a multistage interconnect network capable of dynamic configuration for all switch nodes wherein connections from the first stage expand in space from input connections, and connections to the final stage concentrate in space to output connections or vise versa (See Fig. 2) and

configuration storage (108 mapping tables) at each switch (12 PM) storing a time/space configuration for the switch (See Col. 40, lines 15-31) and all switches dynamically switching configuration to the stored configuration by synchronizing switches of successive stages to a configuration prepare-to-switch signal (select) propagated from at least one switch of an input stage (via the forward channel 32) (See Fig. 21, Col. 22, lines 19-60).

At the time the invention was made, therefore, it would have been obvious to one of ordinary skill in the art to combine McMillen et al. with Sahlman et al. in order to obtain a multi-stage digital cross connect switch and to take advantage of providing mapping tables at each switch node storing a configuration for the switch, all switch nodes dynamically switching configuration to the stored configuration by synchronizing switches of successive stages via the forward channel.

The motivation to do so would have been to provide mapping tables at each switch node storing a configuration for the switch, all switch nodes dynamically switching configuration to the stored configuration by synchronizing switches of successive stages via the forward channel, as suggested by McMillen et al, Col. 22, lines 19-60 and Col. 40, lines 15-31.

Sahlman et al. and McMillen et al. teach substantially all the claimed invention and further "FIG. 2 it is for example possible to connect STM-1 signals from 16 time switches, and correspondingly the outputs to 16 time switches" (See Fig. 2, Col. 5, lines 1-10), but did not disclose expressly the particular application involving limitations of

"each switch comprising a time slot interchanger associated with each input and output port for connection with SONET STS-M frame" .

Ohara teaches a digital cross connection apparatus (10) containing a Time-Space-Time switch construction enabling SONET ST-M frame application (each switch comprising a time slot interchanger associated with each input and output port for connection with SONET STS-M frame) (See Fig. 1, Col. 5, lines 35-41), and

wherein the time slot of the time muxed input are maintained by frame counter output (See Col. 6, lines 25-30).

At the time the invention was made, therefore, it would have been obvious to one of ordinary skill in the art to combine Ohara with Sahlman et al. and McMillen et al. in order to obtain a multi-stage digital cross connect switch and to take advantage of an expandable time slot interchanger at the input and output interface node.

The motivation to do so would have been to accommodate a multi-stage digital cross connect switch and to take advantage of an expandable time slot interchanger at the input and output interface node, as suggested by Ohara in Col. 5, lines 35-41 and Col. 6, lines 25-30.

Regarding claims 38-40, as discussed above, Sahlman et al. further teaches that the connections from a first stage expand in space from input connections and

connections to a different second or final stage concentrate in space to output connections (See Col. 4, line 62 to Col. 6, line 36).

Regarding claims 42-43 and 52, as discussed above, Sahlman et al. further teaches that the connections expand in space from input connections to the first portion, and connections concentrate in space to output connections of the second portion (a SDH frame based time-and-space division switch groups where time switch realizes the rearrangement of the time slots or bytes in accordance with the route selection calculated by the decoder processor control before they are transmitted to the space switch) and response to prepare-t-switch signal (an SDH DXC can transmit traffic between different SDH levels and connect traffic between different signals and the use of the cross connect also includes a possibility for remote control of routing, initialization of reserve routes, connection from one signal to several signals) (See Col. 4, line 62 to Col. 6, line 36).

Regarding claims 44-46, and 47-51, as discussed above, Ohara further teaches that the prepare-to-switch signal is embedded in the second and third bytes of an STS-48 frame (such as A1 byte) (See Col. 5, lines 35-41 30).

Allowable Subject Matter

4. Claims 1-4, 6-20, 22-36, 54 and 57-58 are allowed.

5. Claims 55-56 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and if no art rejection can be applied.

Reason for indicating Allowable Subject Matter

6. The following is a statement of reasons for the indication of allowable subject matter: The prior art along or in combination fails to teach or make obvious the following limitations:

the configuration storage at each switch is configured to store a primary time/space configuration table and a standby time/space configuration table and each switch is configured to switch between the primary and secondary tables in response to the configuration select signal" as recited in the *dependent claim 55-56.*

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Chang whose telephone number is (571) 272-3129. The examiner can normally be reached on Monday - Friday from 8 AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wing Chan can be reached on (571) 272-7493. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

rkc

Richard Chang
Patent Examiner
Art Unit 2616

WING CHAN
SUPERVISORY PATENT EXAMINER